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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,933	12/10/2003	Hung Cai Ngo	AUS920030779US1(4019)	8706

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IBM CORPORATION (JSS)
C/O SCHUBERT OSTERRIEDER & NICKELSON PLLC
6013 CANNON MOUNTAIN DRIVE, S14
AUSTIN, TX 78749

EXAMINER	
LUU, AN T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,933	NGO, HUNG CAI	
	Examiner	Art Unit	
	An T. Luu	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 17-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,8 and 17-24* is/are rejected.

7)☒ Claim(s) *3,5-7,9 and 25-27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12-10-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 4, 8 17-19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by the Lee et al reference (U.S. Patent 6,424,192).

Lee et al discloses in figure 5 an apparatus comprising a multi-phase ring oscillator (multi-feedback CMOS VCO) to generate more than one phases of an oscillator signal Vctrl responsive to an input signal REF; a pulse generator 500 coupled with the multi-phase oscillator to generate a loop clock signal DIVCK, which is a multiple of the oscillator signal and related to the number of phases; and a comparing circuit PFD coupled with the pulse generator to modify the input signal based upon a comparison of the loop clock signal with a reference clock signal REF as required by claims 1 and 4.

As to claim 8, figure 2 discloses a comparison circuit 210 comprising a frequency divider 240 coupled the pulse generator (i.e., including VCO as seen in fig. 5) to generate a feedback control signal having frequency comparable to a frequency associated with the reference clock signal.

As to claim 17, it is rejected for reciting a method/step derived from the apparatus of claim 1 which is rejected as noted above.

As to claim 18, it is inherent that the output clock signal is dynamically adjusting to synchronize with the reference input signal as commonly known in the operation of a phase locked loop circuit.

As to claim 19, it is rejected for reciting a method/step derived from the apparatus of claim 8 which is rejected as noted above.

As to claim 20, it is inherent that pulses are generated based on rising edges of the phases of the oscillating signal since D flip-flop 522 is triggered upon the rising edge of its input signal which is derived from the oscillating signal.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Lee et al reference (U.S. Patent 6,424,192) in view of the JenningsCheck reference (U.S. Patent 5,059,924).

Lee et all discloses all the claimed invention except for teaching an output frequency divider coupled to the pulse generator to dynamically modify the loop clock signal to generate an output clock signal as required by claim 2.

JenningsCheck discloses in figure 1 a phase locked loop circuit (PLL) including, among other thing, an output frequency divider 4 coupled to the output of the PLL for modifying the loop clock signal to generate an output clock signal 12 as required by the claim.

It would have been obvious to one skilled in the art at the time the invention was made to incorporate the teachings of JenningsCheck into that of Lee et al to modify the output of the PLL since a divider is known for modifying a frequency of a clock signal.

A skilled artisan in the art would have been motivated to combine the above references for the purpose of modifying a clock signal to a desired frequency which is suitable for device/component along the processing line.

5. Claims 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Boerstler et al reference (U.S. Patent 6,522,207) in view of the Lee et al reference (U.S. Patent 6,424,192).

Boerstler et al discloses in figures 1 and 5 an apparatus comprising an instruction unit (152 and 156) of an instruction pipeline (i.e., bus connecting I/O to CPU) for performing operations on operands; and a phase locked loop circuit (i.e., within CPU as shown in fig. 5) coupled with the instruction unit to output a pipeline clock signal (i.e., output of PLL) to enable the instruction unit and to synchronized operations performed by the instruction unit with operations performed by other units (i.e., MEM, COMM) along the instruction pipeline as partially required by claim 21.

Boerstler et al does not disclose the phase-locked loop being adapted to generate more than one phase of an oscillator signal responsive to an input signal; to generate a loop clock

signal, which is a multiple of the oscillator signal and related to the number of phases; and to modify the input signal based upon a comparison of the loop clock signal with the reference clock signal.

Lee et al discloses in figure 1 a PLL circuit capable of generating more than one phase of an oscillator signal responsive to an input signal; generating a loop clock signal, which is a multiple of the oscillator signal and related to the number of phases; and modifying the input signal based upon a comparison of the loop clock signal with the reference clock signal as required by claim 21 (See the rejection of claim 1 above).

It would have been obvious to one skilled in the art at the time the invention was made to replace a PLL circuit in Boerstler et al with the one taught by Lee et al since PLL circuit is known to be implemented in many different ways.

A skilled artisan in the art would be motivated to utilize the PLL circuit taught by Lee et al since it is capable of providing a very high frequency (i.e., over 1GHz) having a very low phase noise.

As to claim 22, figure 5 of Boerstler discloses the phase-locked loop circuit comprising an output frequency divider 512 to divide the loop clock signal (K1ref) to generate the pipeline clock signal (Fout).

As to claim 23, the output frequency divider 512 is shown to divide the loop clock signal by a first divisor (K2), the first divisor being based upon a difference in frequency between the reference clock signal and a desired pipeline frequency (i.e., Fout=(K1/K2)Fref).

As to claim 24, figure 5 of Boerstler discloses the phase-locked loop circuit comprising an feedback loop frequency divider 516 to divide the loop clock signal by *another* divisor (i.e., K1) to compare the loop clock signal with the reference clock signal.

Allowable Subject Matter

6. Claims 3, 5-7, 9 and 25-27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to disclose an apparatus comprising elements being configured as recited in claims. Specifically, none of the prior art teaches or fairly suggests, among other things, the following limitations:

- The output frequency divider comprises a output decrementer circuit with an output pulse latch to count transitions of the loop clock signal and transition a voltage latched to an output of the pulse latch between a high voltage and a low voltage to generate the output clock signal as required by claim 3.
- The pulse generator comprises OR gate logic to combine pulses generated in response to a transition of a phase of the more than one phases of the oscillator signal as required by claims 5 and 7.
- The frequency divider comprises a feedback decrementer circuit with a feedback pulse latch to count transitions of the loop clock signal and toggle an output based

upon a count of the transitions, wherein toggling the output generates the feedback signal as required by claims 9 and 25.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to An T. Luu whose telephone number is 571-272-1746. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

An T. Luu
1-15-05

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800